C-BAND 6-BIT GaAs

MONOLITHIC PHASE SHIFTER

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ABSTRACT

The design, fabrication and test result of a GaAs monolithic 6-bit digital controlled phase shifter for use in the 5 to 6 GHz region are described. The chip includes an analog control bit, (0-11°) for phase correction in a closed loop configuration. Less than ±1-degree phase error was achieved on the 11.25°-, 22.5°- and 45°-bits, with ±6-degrees on the 90-degree and 180-degree bits. Over 5 to 6 GHz the return loss was > 15 dB and flatness ±1 dB.

INTRODUCTION

Phased array radars using elemental transceivers will rely on monolithic programmable microwave integrated circuits to achieve minimum size, weight, power consumption and cost. For beam steering programmable phase shifters will be used to adaptively adjust transceiver phase in both the transmit and receiver mode. To achieve maximum effectiveness the sidelobes of the beams must be maintained very low. This requirement imposes severe specifications on the programmed phase shifter accuracy.

This paper reports on the design, fabrication, and test results of a GaAs monolithic phase shifter which contains a 5-bit digital circuit along with an analog circuit bit for fine phase tuning.

Less than ±1-degree phase error was achieved on the 11.25°, 22.5° and 45° bits, with b6-degrees of error on the 90-degree and 180-degree bits. Over the 5 to 6 GHz range, the flatness was ±1 dB, with a return loss of > 15 dB. Temperature testings show small parameter variation with excellent phase tracking from unit to unit. Repeatability and phase shift from chip to chip was extremely uniform.

CIRCUIT TOPOLOGY

The circuit consists of five digital bits, 11.25°, 22.5°, 45°, 90° and 180°; and an analog bit in cascade, as shown in the CALMA layout of Figure 1. The circuits are arranged linearly, proceeding from the analog bit to the smallest bit through the 180-degree bit. The 45-degree bit is positioned between the 90-degree and 180-degree bits to maintain the optimum overall VSWR over 5 to 6 GHz. The overall chip size is 4.19 mm by 9.3 mm with a substrate thickness of 125 μm.

To reduce the overall chip length, the transmission lines are folded with sufficient line spacing maintained to avoid coupling. The Lange couplers are folded to keep the 90-degree and 180-degree bits sizes close to other bit lengths.

All the bits were designed to interface to 50 ohms, so that individual testing of the bits might be easily accomplished. The linear arrangement allows dicing the indvidual bits for comparative measurements.

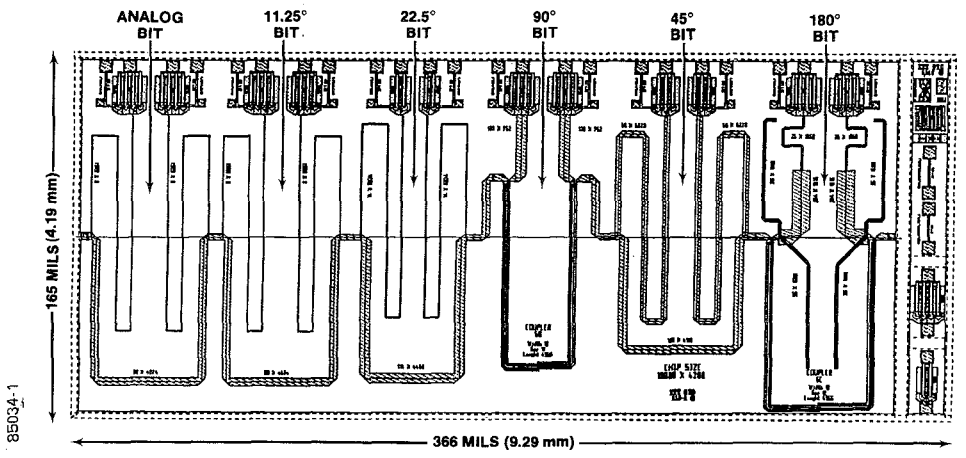

Figure 1. GaAs Monolithic Phase Shifter Layout

The switching FETs are arranged along the edge to accommodate the control leads from the chip and to allow short ribbon ground connections to the FET source pads. The next iteration will include VIA holes for grounding for more uniform construction. All FET bias connections are made through resistors for RF isolation and are individually brought out to pads. The circuits are completely dc coupled. No capacitors are used on the chip. The total gate periphery of the 12 FET switches is 20.4 mm.

CIRCUIT DESCRIPTION

The 11.25°, 22.5° and 45° and bits consist of loaded line sections, while the 90-degree and 180-degree bits use Lange couplers for reflection type phase shifters. The FET size for each bit was optimized for best VSWR and insertion loss, resulting in three different FET peripheries in the circuit: 1200 μm, 1800 μm and 2400 μm. These large FETs also give rise to higher power handling capability.

The analog bit consists of an 11.25-degree bit which uses the FETs in a variable impedance mode to adjust the phase shift over 0-11 degrees. The loaded line sections consists of approximate quarter-wave along transmission lines of about 50 ohms, loaded at both ends with high impedance stubs terminated with the FET switches.

The reflection type 90-degree and 180-degree bit phase shifters employ Lange couplers designed using transmission 12 μm line widths and gaps, and an overall length of 4.96 mm. A 2400 μm FET switch terminates a transmission line matching network, which produces reflected incoming signals with the required 90-degree or 180-degree phase shift.

Accurate modeling of all the circuit elements and discontinuities was used in the design.

A sophisticated model of the FET consisting of a 7-element RLC network is used in the computer analysis and optimization program. Transmission line losses and all discontinuities such as bends, tee junctions and abrupt widths steps are taken into account in the design.

Each phase shift bit was designed and optimized on an individual basis to have > 15 dB return loss so that modeling the entire phase shifter on the computer would not be necessary. The return loss of the loaded line bits gets progressively worse as the required phase shift increases. The 45-degree bit which has the poorest return loss was placed between the 90-degree and 180-degree shifters which typically have excellent return losses due to the Lange couplers.

FABRICATION

The circuits were manufactured using the standard GTC process for Ion-Implanted GaAs. The process includes the Au Ge/Ni metalization of ohmic contacts, 1 μm Cr-Au Schottky gates and air bridges on a 125-μm thick GaAs substrate. A photograph of the completed chip appears in Figure 2.

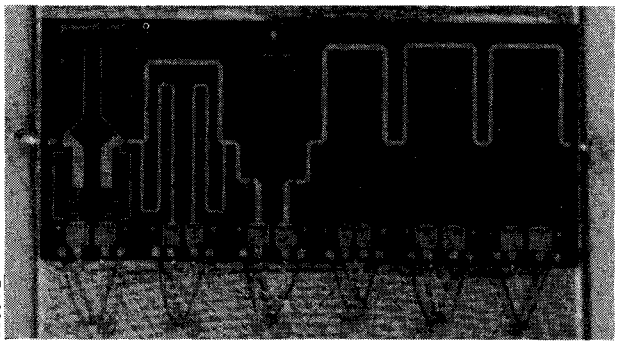

Figure 2. Phase Shifter Substrate

MEASURED PERFORMANCE

Test results for the first iteration 6-bit phase shifter design showed excellent conformity to the design values for all the bits. Table I shows the test results for phase shift, insertion loss difference, and return loss over the 5 to 6 GHz band.

The complete chip insertion loss was measured to be 9.5 dB with a maximum loss variation of ±1 dB over all phases.

Phase and amplitude tracking was measured on several chips over the temperature range of −55°C to +80°C. The worst case deviation from chip to chip was ±10 degrees phase and ±0.5 dB maximum amplitude.

Table I. Test Results

BIT	Phase Shift degrees	Return Loss dB	Insertion Loss Dif dB
11.25	12 ± 1	>19	<1
22.5	21 ± 1	>18	<1
45	44 ± 1	>15	<1
90	95 ± 6	>17	<1
180	170 ± 6	>17	<1
Analog	0 to 11° 0 to -3 Volts	>19	<1

CONCLUSION

A complete C-band 5-bit phase shifter with an analog control fine-tune bit has been built and tested in monolithic form. High phase accuracy with good chip-to-chip phase tracking over −55°C to +80°C has been demonstrated.